PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ko et al.

Serial No.: 09/711,324

Filed: November 13, 2000

For: ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY

Examiner: K. Chen

Group Art Unit: 1765

Attorney Docket No.: 3526.4US (97-1136.4)

NOTICE OF EXPRESS MAILING

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. The listed documents are from co-pending application Serial No. 09/610,049, filed July 5, 2000. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other

possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

DOCUMENTS

U.S. Patent Documents

U.S. Patent No.	Issue Date	Inventor
5,828,096	10/1998	Ohno et al.
5,831,899	11/1998	Wang et al.

Other Documents

Wolf, Stanley, "Silicon Processing for the VLSI Era," cover pages and pages 194-195, Volume 2: Process Integration.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the final Office Action under 37 C.F.R. § 1.113, but before payment of the issue fee. I hereby certify that no item of information contained in the Supplemental Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the statement, therefore no fee pursuant to 37 C.F.R. § 1.17(i) is required.

Respectfully submitted,

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Date: January 3, 2002
BGP/hlg:djp
Enclosures: Form PTO-1449
Copy of documents cited
N:\2269\3526.4 Supplemental IDS.wpd

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
3526.4US (97-1136.4)	09/711,324
Applicant **Ko et al.**	
Filing Date **November 13, 2000**	Group Art Unit **1765**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,828,096	10/1998	Ohno et al.			
	5,831,899	11/1998	Wang et al.			

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		Wolf, Stanley, "Silicon Processing for the VLSI Era," cover pages and pages 194-195, Volume 2: Process Integration.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.